# 零基础学FPGA (二十五)

# 一路走来 ： SDR SDRAM （架构篇）

# 设计报告

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#### 1.1 SDR SDRAM 上电初始化

###### 1.1.1 SDRAM上电初始化架构图

clk\_50m

clk clk\_50m

clk\_100m

rst\_n sdram\_clk

sys\_rst

PLL

clk\_100m

sdram\_clk

sys\_rst

clk\_100m

init\_state

sdram\_cs\_n

sdram\_ras\_n

sdram\_cas\_n

sdram\_cke

sdram\_we\_n

sdram\_ba[1:0]

sdram\_addr[11:0]

clk

rst\_n

sys\_addr[21:0]

clk init\_state

rst\_n

sdram\_init\_done

sdram\_cs\_n

sys\_rst

sdram\_ras\_n

sdram\_cas\_n

Sdram\_init\_FSM

sdram\_cke

sdram\_we\_n

Sdram\_ctrl

sdram\_ba[1:0]

sdram\_addr[11:0]

clk\_100m

sys\_rst

sys\_addr

Sdram\_cmd

sdram\_top

###### 1.1.2 SDRAM上电初始化状态转移图

`end\_trp !=1

Delay\_200us !=1

`end\_tmrd =1\_\_\_\_\_\_\_

Sdram\_cmd\_r =10111

Init\_done = 1

Rst\_n =0

Sdram\_cmd\_r =10111

Init\_done = 0

\*\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r =10111

`end\_tmrd !=1

`end\_trfc8 =1\_\_\_\_\_\_\_

Sdram\_cmd\_r =10111

sdram\_ba\_r <= 2'b00; sdram\_addr\_r <= {

2'b00, //模式寄存器设置A11,A10

1'b0, //A9，设置为突发读/突发写

2'b00, //A8，A7

3'B011,//CAS潜伏期设置为个单位周期

1'b0, //A3,突发传输方式设置为”顺序"

3'b011 //突发长度设置，设置为8

};

`end\_trfc8 !=1

\*\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r =10111

`end\_trfc1 =1\_\_\_\_\_\_\_

Sdram\_cmd\_r =10001

`end\_trfc1 !=1

\*\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r =10111

\*\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r =10111

`end\_trp =1\_\_\_\_\_\_\_\_

Sdram\_cmd\_r =10001

Delay\_200us =1\_\_\_\_\_\_

Sdram\_cmd\_r =10010

#### 1.2 SDRAM 自刷新

#### 1.2.1 SDRAM 自刷新架构图

work\_state

sdram\_cs\_n

sdram\_ras\_n

sdram\_cas\_n

sdram\_cke

sdram\_we\_n

clk

rst\_n

clk

rst\_n work\_state

init\_done

sdram\_ref\_req sdram\_ref\_ack

clk\_100m

sys\_rst

sdram\_cs\_n

init\_done

sdram\_ras\_n

sdram\_cas\_n

sdram\_work\_FSM

sdram\_cke

sdram\_we\_n

clk\_100m

clk

rst\_n sdram\_ref\_req

sys\_rst

Sdram\_cmd

clk\_100m

timer

sys\_rst

Sdram\_ctrl

clk\_50m

clk\_100m

clk clk\_50m

clk\_100m

rst\_n sdram\_clk

sys\_rst

PLL

sdram\_clk

sys\_rst

#### 1.2.2 SDRAM 自刷新状态转移图

`end\_trfc !=1

\*\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10111

sdram\_ref\_ack = 1

sdram\_ref\_req=1\_\_\_\_

Sdram\_cmd\_r = 10001

Sdram\_cmd\_r =10111

Init\_done = 1

\*\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10111

#### 1.3 SDRAM 读写状态

###### 1.3.1 SDRAM 读写状态转移图

work\_state

sdram\_cs\_n

sdram\_ras\_n

sdram\_cas\_n

sdram\_cke

sdram\_we\_n

sdram\_ba[1:0]

sdram\_addr[11:0]

clk

rst\_n

clk

rst\_n work\_state

init\_done

sdram\_rd\_req

sdram\_wr\_req

sdram\_rd\_ack

sdram\_wr\_ack

sdram\_cs\_n

clk\_100m

sdram\_ras\_n

sys\_rst

sdram\_cas\_n

init\_done

sdram\_cke

sdram\_rd\_req

sdram\_we\_n

sdram\_wr\_req

wr\_req

sdram\_ba[1:0]

sdram\_rd\_ack

sdram\_addr[11:0]

sdram\_wr\_ack

sys\_rst

clk\_100m

sdram\_work\_FSM

sdram\_cmd

work\_state

sys\_data\_in[15:0]

sdram\_data[15:0]

clk

rst\_n

sys\_data\_out[15:0]

sys\_data\_in[15:0]

sdram\_data

clk\_100m

sdram\_wr\_data

sys\_rst

sdram\_TOP

sys\_data\_out[15:0]

sdram\_clk

clk\_50m

clk\_100m

clk clk\_50m

clk\_100m

rst\_n sdram\_clk

sys\_rst

PLL

sys\_rst

###### 1.3.2 SDRAM 读写状态转移图

`end\_trwait !=1

`end\_trd !=1

`end\_tcl !=1

`end\_trd =1\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10111

`end\_tcl =1\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10111

\*\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10111

`end\_trcd =1

Sys\_wr\_wn = 1\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10101

sdram\_ba\_r <= sys\_addr[21:20];

sdram\_addr\_r <= {

4'b0100, //设置A10为1，写完成允许自动预充电sys\_addr[7:0] //列地址

}

};

`end\_trwait =1\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10111

`end\_trcd !=1

\*\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10111

Sdram\_wr\_req = 1 | sdram\_rd\_req = 1

Sdram\_cmd\_r = 10011

sdram\_ba\_r <= sys\_addr [21:20]; //L-bank有效

sdram\_addr\_r <= sys\_addr[19:8]; //发行地址

Sdram\_cmd\_r =10111

Init\_done = 1

`end\_trcd =1

Sys\_wr\_wn = 0\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10100

sdram\_ba\_r <= sys\_addr[21:20];

sdram\_addr\_r <= {

4'b0100, //设置A10为1，写完成允许自动预充电sys\_addr[7:0] //列地址

}

};

`end\_tdal =1\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10111

`end\_tdal!=1

`end\_twrite =1\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10111

\*\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Sdram\_cmd\_r = 10111

`end\_trcd !=1

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